Vojin G. Oklobdzija, Ph.D., IEEE Life Fellow
Professor Emeritus, University of California
(Phonetic spelling: Vo-in Oklob-j-a)
Past-President, IEEE Circuits and Systems Society, 2014, 2015



Contact:

Address:
1285 Grizzly Peak Blvd, Berkeley, CA 94708

Telephone and email:
510-230-3267; vojin@ieee.org, vojin@acsel-lab.com, vojin@integration-corp.com

---

Expertise

- Computer System Design and Computer Architecture
- VLSI Circuits and Systems
- System Clocking and Clocked Storage Elements
- Logic Design and Machine Organization
- Low-Power Design and Technology
- Computer Arithmetic: VLSI adders, multipliers arithmetic, crypto processors
- Microprocessor Design
- Design for Testability and Fault-Tolerant Computer Design

Professional Summary

Expert witness with 25 years of experience, provided testimony in civil jury trial, and ITC court in Washington. Testimony to the judge (Hong Kong) Ltd. JAMS Arbitration No. 1220062943. Provided deposition testimonies, written over 30 expert reports on infringement, claim construction, participated in patent review.
Over 50 years of experience in computer and semiconductor industry and 35 years of consulting experience for most major computer and semiconductor companies in the USA and abroad.
Twenty years in academic position, reaching the highest Full Professor level in five years and IEEE Fellow, followed by IEEE Life Fellow (highest) level in engineering profession.

Litigation Support Experience:

Summary:

Court testimonies:

(a) ***International Trade Commission (ITC)***, Washington, D.C., June 2013.
(b) ***Northern California District Court***, San Jose California. (I was the only expert on the side of TPL against half-dozen experts on the side of HTC). Three days of testimony, one week in court. Case won October 2, 2013.
(c) Tutorial to the Judge in the United States District Court, Western District of Texas, Austin Division, August 22, 2019.
(d) Testimony to the judge (Hong Kong) Ltd. JAMS Arbitration No. 1220062943.

Depositions:

Given over 20 deposition testimonies. Most recent 3 depositions in 2025.

References:

Available upon request.

Education: Vojin G. Oklobdzija

Year	College/University	Degree
1982	University of California at Los Angeles	Ph.D., in Computer Science with Minor in Electronics
1978	University of California at Los Angeles	MS, Computer Science with thesis in Computer Arithmetic
1971	University of Belgrade, Yugoslavia	Ms. E.E. (Dipl. Ing) Electronic and Telecommunications
1968	University of Belgrade, Yugoslavia	BS. E.E. (Ing) Electrical Engineering
1967-1973	Dept. of Physics, Univ. of Belgrade	Physics, Graduate study in Physics

Professional Associations and Achievements

- Fellow of the Institute of Electrical and Electronic Engineers, since 1996[1].
- Life Fellow, IEEE since 2016[2].
- Member, Japan IEICE Society.
- Fulbright Scholar 1976.
- Fulbright Professor, Peru 1991.
- Fulbright Professor, Argentina, 2013.
- President: IEEE Circuits and Systems Society (2014-2016 two-year term).
- President Elect, IEEE Circuits and Systems Society (2013).
- Vice President, Technical Activities, IEEE Circuits and Systems Society (2009-2013).
- Board of Governors, IEEE CAS, 2010-2016.

Award and Recognitions

Fulbright Scholarship, 1976-77.
National Science Fellowship, Plasma Physics, 1971-73.
IBM patent award, 1985.
IBM invention plateau award, 1985.
Best Paper Award in Computer Architecture track, HICSS-88.
Fulbright Professorship, 1990. Peru, South America.
Fulbright Professorship, 2013. Argentina.
N. Price Fellowship in Electrical Engineering, Australia 1993.
Fellow IEEE, 1995.
Distinguished Lecturer of IEEE Circuits and Systems Society.
Distinguished Lecturer of IEEE Solid-State Circuits Society.
Outstanding Academic Title, "Computer Engineering Handbook," CRC Press 2002.
Listed in Marquis: "Who'sWho in America," "Who'sWho in Science and Engineering,"
"Clock-Powered Circuits Set Efficiency Record," Electronic Engineering Times, December 1, 1997.
"ISLPED '97 Shows What's Up in Ultra-Low Power Digital Systems," article mention, Electronic Design, August 4, 1997.
Active Ham-Radio operator, since 1962. Call sign WF1A, holder of the highest class.[3]

[1] only less than 0.1% of 427,000 members are elected IEEE Fellows each year.
[2] the highest achievable grade, there are only 3517 total out of 427,000 members in the world.
[3] Experimenting with packet radio networks, low-power signal propagation, antennas, computer-radio interfaces.

Current and Past Professional Service:

- Past-President, IEEE Circuits Systems Society
- General Chair: International Symposium on Computer Arithmetic, ARITH-20. (Tubingen, Germany, 2011)
- General Chair: Int'l Symposium on Low-Power Electronics Design, Austin, Texas, 2010.
- Technical Program Chair, Int'l Symposium on Low-Power Electronics Design, Bangalore, 2009.
- Technical Program Chair: International Symposium on Low-Power Electronics, 2008.
- Editor, Computer Engineering Series, Taylor & Francis.
- Editorial Board Taylor and Francis / CRC Press.
- Associate Editor, IEEE Transactions on Computers: 2001-2005,
- Associate Editor, IEEE Transactions on VLSI Systems: 1995-2003,
- Associate Editor, IEEE Transaction on Circuits and Systems II: 2006-2008.

U.S. Patents: Vojin G. Oklobdzija

Patent Number	Date Issued	Title
20230087096-A1	3/23/2023	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE AND TEMPERATURE (PVT) VARIATIONS
20230045265-A1	2/09/2023	FAST CLOCKED STORAGE ELEMENT
20230015430-A1	1/19/2023	FLOATING-POINT ACCUMULATOR
11,558,041 B1	1/17/2023	FAST CLOCKED STORAGE ELEMENT
20230004353-A1	1/5/2023	FLOATING POINT ACCUMULATER WITH A SINGLE LAYER OF SHIFTERS IN THE SIGNIFICAND FEEDBACK
20220308834-A1	9/29/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
11442696-B1	9/13/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
11,429,349 B1	8/30/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH CARRY-SAVE ACCUMULATOR
11411553-B1	8/9/2022	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE AND TEMPERATURE (PVT) VARIATIONS
11366638	06/21/2022	FLOATING POINT MULTIPLY – ADD, ACCUMULATE UNIT WITH COMBINED ALIGNMENT CIRCUITS
11,442,696	11/23/2021	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
10,707,839	07/07/2020	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE, AND TEMPERATURE (PVT) VARIATIONS
7,509,486	03/24/2009	ENCRYPTION PROCESSOR FOR PERFORMING ACCELERATED COMPUTATIONS TO ESTABLISH SECURE NETWORK SESSIONS CONNECTIONS

6,753,715	06/22/2004	SYSTEM FOR SYMMETRIC PULSE GENERATOR FLIP-FLOP
20040057313-A1	3/25/2004	SYSTEM FOR SYMMETRIC PULSE GENERATOR FLIP-FLOP
6,693,459	02/17/2004	METHOD AND SYSTEM FOR IMPROVING SPEED IN A FLIP-FLOP,"
6,647,487	11/11/2003	METHOD AND SYSTEM FOR REDUCING HAZARDS IN A FLIP-FLOP
6553541-B1	4/22/2003	REDUCED-COMPLEXITY SEQUENCE DETECTION
20030062940-A1	4/3/2003	METHOD AND SYSTEM FOR REDUCING HAZARDS IN A FLIP-FLOP
20030062925-A1	4/3/2003	METHOD AND SYSTEM FOR IMPROVING SPEED IN A FLIP-FLOP
20030056129-A1	3/20/2003	CONDITIONAL PRE-CHARGE METHOD AND SYSTEM
20020143841-A1	3/10/2002	MULTIPLEXER BASED PARALLEL N-BIT ADDER CIRCUIT FOR HIGH SPEED PROCESSING
6,353,843	03/05/2002	HIGH PERFORMANCE UNIVERSAL MULTIPLIER
6,301,599	10/09/2001	MULTIPLIER CIRCUIT HAVING OPTIMIZED BOOTH ENCODER/SELECTOR
6,282,556	08/28/2001	HIGH PERFORMANCE PIPELINED DATA PATH FOR A MEDIA PROCESSOR
6,243,728	06/05/2001	PARTITIONED SHIFT RIGHT LOGIC WITH ROUNDING SUPPORT
6,232,810	05/15/2001	FLIP-FLOP
6,128,641	10/03/2000	DATA PROCESSING UNIT WITH HARDWARE ASSISTED CONTEXT SWITCHING CAPABILITY
4,992,398	02/12/1991	INSTRUCTION CONTROL MECHANISM FOR A COMPUTING SYSTEM WITH REGISTER RENAMING AND QUEUES INDICATING AVAILABLE REGISTERS
4,847,759	07/11/1989	REGISTER SELECTION MECHANISM AND ORGANIZATION OF AN INSTRUCTION PREFETCH BUFFER
4,714,994	12/22/1987	INSTRUCTION PREFETCH BUFFER CONTROL
4,700,086	10/13/1987	CONSISTENT PRECHARGE CIRCUIT FOR CASCODE VOLTAGE SWITCH LOGIC

Litigation Support Experience:

Summary:

Court testimonies:

(a) ***International Trade Commission (ITC)***, Washington, D.C., June 2013.
(b) ***Northern California District Court***, San Jose California. (I was the only expert on the side of TPL against half-dozen experts on the side of HTC). Three days of testimony, one week in court. Case won October 2, 2013.
(c) Tutorial to the Judge in the United States District Court, Western District of Texas, Austin Division, August 22, 2019.
(d) Testimony to the judge (Hong Kong) Ltd. JAMS Arbitration No. 1220062943.

Depositions:

Given over 20 deposition testimonies. Most recent 3 depositions in 2025.

References:

Available upon request.

Date:	2022-25	**Hagens Berman Sobol Shapiro LLP, Bathaee Dunne LLP**
	Case:	*Day v. Advanced Micro Devices, Inc., Case No. 3:22-cv-04305-VC and Pietosi v. HP, Inc., Case No. 3:22-cv-04273-CRB*
	Parties:	*Day v. Advanced Micro Devices, Inc., Case No. 3:22-cv-04305-VC and Pietosi v. HP, Inc., Case*.
	Project:	*To render an opinion where Counsel has requested an opinion*
	Represent:	*Pietosi and Day*
	Subject:	Defective product
	Status:	*Deposition* on Feb. 3, 2025.
Date:	2022-25	**Devlin Law Firm LLC**
	Case:	Ocean Semiconductor LLC, v. *Analog Devices, Inc. C.A. No. 1:20-cv-12310-PBS*
	Parties:	Ocean Semiconductor LLC, *Plaintiff,* v. *Analog Devices, Inc. Defendant.*
	Project:	Claim infringement of U.S. Patent No.6,836,691
	Represent:	Ocean Semiconductor LLC
	Subject:	U.S. Patent Nos. 6,420,097, 6,660,651, 6,725,402, 6,907,305, 6,968,248, 8,120,170, 8,847,383, 7,080,330, 6,836,691, and 8,676,538 Additional reexam response Ocean Semiconductor LLC, v. Western Digital
	Status:	*Two depositions* on Dec.11 and Dec.13, 2025
Date:	2022-24	**Hundel Law Group**
	Case:	*VOIP-PAL.com, Inc. vs. Amazon.com, Inc.; Verizon Communications, Inc.; T-Mobile US, Inc., in the United States District Court for the Western Division of Texas, Waco Division, Civil Action No. 6:21-cv-668-A*
	Parties:	VOIP-PAL.com, Inc. vs. Amazon.com, Inc.; Verizon Communications, Inc.; T-Mobile US, Inc.
	Project:	Consultant on the patent infringement. Writing 6 expert reports. *Three depositions: April-May, 2023*.
	Represent:	VOIP-PAL.com, Inc.
	Subject:	Patent infringement
	Status:	Pending.
Date:	2023-24	**Covington & Burling LLP**
	Case:	*Samsung Electronics Co., Ltd. et al. v. Netlist, Inc., No. 1:21-cv-01453 (D. Del.)*
	Parties:	Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.
	Project:	Consulting expert.
	Represent:	Samsung Electronics Co., Ltd.
	Subject:	Consultation and prior art search.
	Status:	Closed.
Date:	2023	**Jones Day**

Case: Consultant in connection with the preparation and prosecution of an inter partes review petition
Parties: Qualcomm/ARM PTAB Matters
Represent: Qualcomm Inc.
Subject: Consultation regarding patents, prior art, and other relevant aspects of the technology at issue in these matters.
Status: Closed.

Date: 2023 **Knobbe, Martens, Olson & Bear, L.L.P**
Case: Representing Qualcomm Inc. ("Qualcomm") in inter partes review proceedings at the United States Patent & Trademark Office
Parties: Qualcomm Inc., United States Patent & Trademark Office
Represent: Qualcomm Inc.
Subject: Inter partes review proceedings at the United States Patent & Trademark Office.
Status: Closed.

Date: 2023 **Simon Law Group**
Case: *Kelly Schwalbach, an individual vs. VNA Hospice and Palliative Care of Southern California; Sunbeam Products, nc.; Walmart Inc.; Claremont Lincoln University; Superiour Court of the State of California for the County of Los Angeles – Pomona Courthouse South, Case No.: 18STCV00634*
Parties: Kelly Schwalbach vs. VNA Hospice and Palliative care et al.
Represent: Forensic examination of the product. Expert report. *Deposition* on August 14, 2023.
Subject: Successfully settled, October 2023.

Date: 2021-23 **Winston & Strawn LLP** (lead attorney: Michael Rueckheim, James Lin)
Case: *Netlist, Inc. v. Micron Technology, Inc. et al.* (Case No. 6:21-cv-430 and -431), currently pending in the U.S. District Court for the Western District of Texas and conduct of inter partes review (IPR) proceedings before the U.S. Patent Office, Patent Trial and Appeal Board
Parties: Netlist, Inc. v. Micron Technology, Inc. et al.
Project: Netlist, Inc. v. Micron Technology, Inc. et al. (Case No. 6:21-cv-430 and -431), U.S. District Court for the Western District of Texas.
Represent: Micron Technology, Inc.
Status: Consultation regarding patents, prior art, and other relevant aspects of the technology at issue in these Matters.
Status: unknown

Date: 2021 **Dhillon Law Group Inc.** (attorney: Nitoj P. Singh)
Case: *Cryplex Inc. v. Bitmain Technologies Holding Company, Superior Court of California – Santa Clara County, Case No. 18CV337836.*
Parties: Cryplex Inc. v. Bitmain Technologies Holding Company.
Project: Identifying proprietary technology of Cryplex Inc.
Represent: Cryplex Inc.
Status: Trade secret infringement project.
Status: Ongoing.

Date: 2021 **Cesari and McKenna, LLP**

Case: *WildlifeAcoustics, lnc. v. FrontierLabs PTY., Ltd,* l:20-cv-10620(GAO) (D. Mass.)
Parties: SRC LLC v. Intel Corp.
Project: Consulting services in connection with Frontier's litigation involving Wildlife Acoustics, Inc.
Represent: Frontier Labs PTY., Ltd.
Subject: Opinions and analysis relating to non-infringement of Frontier's accused products, including Expert Declaration.
Status: Closed.

Date: 2020 **Di Muro Ginsberg, P.C.**
Case: *Case No. 3:17-cv-00561-WHO, United States District Court, Northern District of California.*
Parties: SRC LLC v. Intel Corp.
Project: Expert in the Inter Partes Review dispute between SRC, and Intel Corp.
Represent: SRC LLC
Subject: Patent review.
Status: Closed.

Date: 2020 **Weeks Nelson LLP.**
Case: *Red Hydrogen LLC v. CloudMinds (Hong Kong) Ltd. JAMS Arbitration No. 1220062943.*
Parties: Red Hydrogen LLC v. CloudMinds (Hong Kong) Ltd.
Project: Expert opinion on manufacturing process of mobile phone.
Represent: Red Hydrogen LLC, Testimony to the judge (Hong Kong) Ltd. JAMS Arbitration No. 1220062943
Subject: Mobile phone manufacturing.
Status: unknown

Date: 2019 **Freitas & Weinberg LLP.**
Case: *Aquila Innovations, Inc. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00554; Polaris Innovations Ltd. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00555 and Collabo Innovations, Inc. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00552*.
Parties: Aquila Innovations, Inc., Polaris Innovations Ltd. Collabo Innovations, Inc. v. Advanced Micro Devices.
Project: Three expert reports, rebuttal on expert report, tutorial to the Judge in the United States District Court, Western District of Texas, Austin Division, given on August 22, 2019.
Represent: Aquila Innovations, Inc, Polaris Innovations Ltd., Collabo Innovations, Inc.
Subject: Patent infringement.
Status: Unknown, presumed settled.

Date: 2019 **Antonelli, Harrington & Thompson LLP.**
Case: American Patents LLC v MediaTek et al. (6:18-cv-339) and
American Patents LLC v. Analog Devices, Inc. et al. (6:18-cv-356). in The United States District Court for the Western District of Texas Waco Division.
Parties: *American Patents LLC. v. MediaTek et al.and Analog Devices, Inc.*

	Project:	Patent examination, claim construction, claim construction answering brief.
	Represent:	American Patents LLC
	Subject:	Patent infringement
	Status:	Unknown
Date:	2018	**Morrison & Foerster LLP.**
	Case:	Case No. 3:17-cv-00561-WHO, United States District Court, Northern District of California.
	Parties:	*Synopsys, Inc. v. Ubiquiti Networks, Inc., et al.*
	Project:	Expert opinion on the Synopsys tool usage, *two expert reports*, *deposition testimony given, on August 31, 2018*.
	Represent:	Ubiquiti Networks, Inc..
	Subject:	Synopsys tool usage.
		Settled
Date:	Nov. 2017	**Akerman LLP**
	Case:	Qbex Computadores, S.A. v. Intel Corporation, Case No. 5:17-cv-03375-SVK, United States District Court, Northern District of California, San Jose Division
	Parties:	Qbex Computadores, S.A. v. Intel Corporation. (defendant)
	Project:	Representing Qbex Computadores, S.A. in case of overheating mobile phones. Performing reverse engineering and forensic analysis.
	Status:	inactive since 2018
Date:	2017	**Swanson & Bratschun LLC.**
	Case:	Inter Parties Review Cases.
	Parties:	*Amazon.com, Inc. v. Avago Technologies General IP.*
	Project:	Reviewing patents, examining prior art, Inter Partes Review of various patents.
	Represent:	Avago Technologies.
	Subject:	Client – Server technology
	Status:	Settled.
Date:	2017	**Bunsow de Mory LLP.**
	Case:	Case Nos. 3:12-cv-03865, -03876, -03877, -03880, -03881 (N.D. Cal.)
	Parties:	*Technology Properties Limited LLC et al v. Huawei Technologies Co., Ltd.*
	Project:	Independent, *expert opinion on the patent*, claim construction, prior art.
	Represent:	Technology Properties Limited LLC et al.
	Subject:	Chip clocking
	Status:	Settled.
Date:	2016-2017	**Freitas Angell & Weinberg LLP**
	Case:	In the matter of Broadcom Corporation and Avago Technologies
	Parties:	*Broadcom and Avago vs Amazon*
	Project:	Patent examination, prior art examination,
	Status:	Settled 2017
Date:	2015-2106	**Desmarairs LLP.** (Attorney Sean T. Doyle)
	Case:	Civil Action No. 1:13-cv-00453-SLR
	Parties:	*Intellectual Ventures LLC vs. Toshiba Corp.*

Project: *Independent, expert opinion on the infringement*, patent, claim construction, invalidity contentions, writing expert report.
Represent: Intellectual Ventures LLC.
Subject: Processor on-chip testability, debugging and service.
Status: **Settled.**

Date: 2015-2106 **Farney Daniels PC**
Case: *Apple Inc., HTC Corp., HTC America Inc., Samsung Electronics Co. LTD and Samsung Electronics America Inc., Amazon.com Inc., v. Memory Integrity LLC*, USDC, Richmond, Virgina, Case: IPR2015-00163.
Parties: Apple Inc., HTC Corp., HTC America Inc., Samsung Electronics Co. LTD and Samsung Electronics America Inc., Amazon.com Inc., v. Memory Integrity LLC.
Project: Independent, *expert opinion on the litigation*, patent, *claim construction* etc. *Two deposistion testimonies: Nov. 24, 2015 and Jan. 8, 2016.*
Represent: Memory Integrity LLC., Patent Owner.
Subject: Cache coherency mechanism in multiprocessor system
Status: Settled 2016.

Date: 2015 **Latham and Watkins LLP**
Case: *Samsung Electronics Co. LTD and Samsung Electronics America Inc.*, *v. Nvidia Corp.,Old Micro Inc., F/K/A Velocity Micro Inc,.and Velocity Holdings, LLC,* USDC, Richmond, Virgina, CIVIL ACTION NO. 3:14-cv-00757-REP
Parties: Samsung Electronics Co. LTD and Samsung Electronics America Inc., Nvidia Corp. Old Micro Inc., F/K/A Velocity Micro Inc, and Velocity Holdings, LLC.
Project: Independent, *expert opinion on the litigation, patent, claim construction* etc. *Deposition testimony: October 29, 2015.*
Represent: Nvidia Corp., defendant.
Subject: Display power down technology
Status: Case settled

Date: 2015 **Nelson Bumgardner P.C.**
Case: *Technology Properties LTD. LLC, v. Barnes and Noble Inc. and Technology Properties LTD. LLC, Phoenix Digital Solutions LLC and Patriot Scientific Corp. vs. LG Electronics Inc. and LG Electronics USA Inc.*, USDC, N.D. Cal., Case No.: 3:12-CV-03863-VC, and Case No. 3:12-cv-03880-VC (PSG).
Parties: Technology Properties LTD. LLC, v. Barnes and Noble Inc. and Technology Properties LTD. LLC, Phoenix Digital Solutions LLC and Patriot Scientific Corp. vs. LG Electronics Inc. and LG Electronics USA Inc.
Project: Independent, *expert opinion on the patent, claim construction*, testifying services etc.
Represent: Technology Properties LTD. LLC.
Subject: Microprocessor clocking
Status: Case settled

Date: 2015 **Arnold and Porter LLP**
Case: *Synopsys Inc. v. Atop Tech Inc.*, USDC, N.D. Cal., Civil Case: No 3:13-cv-02965-MMC.

Parties: Synopsys Inc. v. Atop Tech Inc.
Project: *Independent, expert opinion on the patent*, testifying services etc.
Represent: Atop Tech Inc.
Subject: IC timing simulation, CAD.
Status: unknown

Date: 2015 **AZA Law**
Case: *Parthenon Unified Memory Architecture, v. HTC Corporation and HTC America Inc*, USDC, Eastern District of Texas, Marshal Division, Case No. 2:14-cv-00690
Parties: Parthenon Unified Memory Architecture, HTC Corporation and HTC America Inc.
Project: *Independent, expert opinion on the litigation*, patent, *claim construction* etc.
Represent: Parthenon Unified Memory Architecture, plaintiff.
Subject: Mobile phone chip shared memory function
Status: Settled

Date: 2012-14 **Otteson Law Group of Agility IP Law, LLP**
Case: *Acer, Inc., et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00877; *HTC Corporation, et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00882; *Barco NV v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-05398
Parties: Acer, Inc., Acer America Corporation, Gateway, Inc., Barco NV, Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited, HTC Corporation, HTC America, Inc.
Project: Patent infringement dispute related to computer circuits and logic. Study of patents and publications, *preparation of multiple expert reports*. (Transferred from Farella Braun + Martel LLP.)
Represent: Technology Properties Limited
Subject: Microprocessor clocking
Status: Settled, won
Work: ***Four deposition testimonies*** ***2011, 2012, 2013***, Expert Report, Infringement Report, Two days testimony at International Trade Commission Court (June 5,6, 2013). Two weeks in the ITC court.

Court testimonies:

(e) ***International Trade Commission***, Washington, D.C., June 2013.
(f) ***Northern California District Court***, San Jose California. (I was the only expert on the side of TPL against half-dozen experts on the side of HTC). Three days of testimony, one week in court.
(g) Case won October 2, 2013.

Date: 2012 **Wolf Greenfield and Sacks P.C**
Case: *In the Matter of Certain Consumer Electronics and Display Devices and Products Containing Same*, USITC, Inv. No. 337-TA-836 and parallel district court actions *Graphics Properties Holdings, Inc. v. Research In Motion Ltd., et al.,* USDC, D. Del., Case No. CV11-01161 (and related actions CV11-01161, CV11-01162, CV11-01163, CV11-01164, CV11-01165)

Parties: Graphics Properties Holdings, Inc., Research In Motion Ltd., Research In Motion Corp., HTC Corporation, HTC America, Inc., LG Electronics, Inc., LG Electronics, LG Electronics MobileComm U.S.A., Apple Inc., Samsung Electronics Co., Ltd., Samsung Electronics Co. Ltd., Samsung Telecommunications, Sony Corporation, Sony Corporation of America, Sony Electronics, Inc., Sony Ericson Mobile, Sony Ericson Mobile
Project: *Preparing expert witness report*. Assisting in claim construction.
Represent: Graphics Properties Holdings, Inc.
Subject: Microprocessor clocking
Status: Settled: December 2012

Date: 2012 **Irell & Manella LLP**
Case: *Infineon Technologies AG, et al. v. Atmel Corporation*, USDC, D. Del., Case No. CV11-00307
Parties: Infineon Technologies AG, Infineon Technologies North America Corp., Atmel Corporation
Project: *Independent, expert opinion on the litigation, patent, claim construction* etc.
Represent: Atmel Corporation
Subject: Thermal and Power Management of Computer Systems
Status: Settled

Date: 2011 **Arnold and Porter LLP**
Case: *Optimum Power Solutions LLC vs. Hewlett-Packard Company*, USDC, N.D. Cal., Case No. CV12-03125 (transferred from USDC, D. Del., Case No. CV11-00853) (related cases in USDC, N.D. Cal., CV12-03127, CV12-03123, CV12-01509, CV12-03126; related cases in USDC, D.Del., CV11-00854, CV11-00855, CV11-00856)
Parties: Optimum Power Solutions LLC, Hewlett-Packard Company
Project: Patent infringement, search for prior art.
Represent: Hewlett-Packard Company
Subject: IC low-voltage operation, power management
Status: Closed

2009 **DLA Piper US LLP**
Case: *Zoran Corp vs. DTS Inc.*, Superior Court of California, County of Los Angeles, Northwest District, Case No. LC 083529
Parties: DTS Inc., Zoran Corp.
Project: Licensing / product infringement dispute. *Preparing expert witness report, expert testimony, expert rebuttal report*, product infringement investigation.
Represent: Zoran Inc.
Subject: DTS Algorithm, reverse engineering
Status: Settled

Date: 2008-11 **Farella Braun + Martel LLP**
Case: *Acer, Inc., et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00877; *HTC Corporation, et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00882; *Barco NV v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-05398

Parties: Acer, Inc., Acer America Corporation, Gateway, Inc., Barco NV, Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited, HTC Corporation, HTC America, Inc.
Project: Patent infringement case. *Preparing expert witness report*. Assisting in claim construction.
Represent: Technology Properties Limited
Subject: Microprocessor clocking, asynchronous communication, processor architecture
Status: Transferred to another attorney group
Work: *Two deposition testimonies given*, Claim construction, Patent invalidity analysis, Expert report, Prior art search.

Date: 2008-09 **Nixon Peabody LLP / Thelen LLP**
Case: *Technology Properties Limited, et al. v. HTC Corporation, et al.*, USDC, E.D. Tex., Case No. CV08-00174
Parties: Technology Properties Limited, Patriot Scientific Corporation, HTC Corporation, HTC America, Inc., Syrus XM, ASUSTeK Computer, Inc.
Project: Patent infringement case.
Represent: Technology Properties Limited
Subject: Microprocessor architecture, uP clocking
Status: Moved to another attorney firm, 2009, later won the case.

Date: 2008-09 **Townsend Townsend & Crew**
Case: TPL, case filed in Eastern District of Texas
Parties: TPL vs. Patriot Scientific Corporation, HTC Corporation, HTC America, Inc., Syrus XM, ASUSTeK Computer, Inc.
Project: Patent infringement case.
Represent: Technology Properties Limited
Subject: Computer circuits and logic, microprocessor asynchronous clocking
Status: Transferred to other law firms including Farella Braun + Martell, Nixon Peabody LLP / Thelen LLP.
Work: Patent invalidity prosecution assistance given, prior art search.

Date: 2007-08 **Dechert LLP**
Case: Acer, Inc., et al. v. Hewlett-Packard Company, USDC, W.D. Wisc., Case No. CV07-00620
Parties: Acer, Inc., Acer America Corporation, Hewlett-Packard Company
Project: Patent infringement dispute. *Preparing expert report*, product infringement investigation.
Represent: Hewlett-Packard Co.
Subject: Computer circuits and logic, microprocessor asynchronous clocking
Status: Closed

Date: 2007 **Townsend Townsend & Crew**
Case: *Technology Properties Limited Inc., et al. vs. Fujitsu Limited, et al.*, USDC, E.D. Tex., Case No. CV08-00494
Parties: Technology Properties Limited, Inc., Patriot Scientific Corporation, Fujitsu Limited, Fujitsu General America, Inc., Fujitsu Computer Products of America, Inc., Fujitsu Computer Systems Corp., Fujitsu Microelectronics America, Inc., Fujitsu Ten Corporation of America, Matsushita Electrical Industrial Co., Ltd.,

Panasonic Corporation of North America, JVC Americas Corporation, NEC Corporation NEC Electronics America, Inc., NEC America, Inc., NEC Display Solutions of America, Inc., NEC Solutions America, Inc., NEC Unified Solutions, Inc., Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronics Components, Inc., Toshiba America Information Systems, Inc., Toshiba America Consumer Products, LLC, NEC Corporation of America, ARM Inc., ARM Ltd.

Project: Patent infringement dispute related to computer circuits and logic. Study of patents and publications, *preparation of expert reports*, assisting in a deposition.
Represent: Technology Properties Limited Inc.
Subject: Computer circuits and logic, microprocessor asynchronous clocking
Status: Closed

Date: 2004-06 **Kellogg, Huber Hansen Todd & Evans PLLC**
Case: OKI America, Inc. v. Advanced Micro Devices Inc., USDC, N.D. Cal., Case No. CV04-03171
Parties: OKI America, Inc., OKI Electric Industry Company, Ltd., OKI Data Corporation, OKI Data Americas, Inc., OKI Telecom, Inc., Advanced Micro Devices Inc., Pankaj Dixit,
Project: Preliminary patent invalidity contention. *Writing expert report*. *Deposition testimony*.
Represent: OKI plaintiffs
Subject:
Status: Closed

Date: 2005 **Irell & Manella LLP**
Case Examining Patent, No: 6,126,235. Contact attorney: Rudy Y. Kim
Project: Patent examination.
Represent:
Subject:
Status: Closed

Date: 2004 **Arent Fox Kintner Plotkin & Kahn, PLLC:**
Case *Hitachi Ltd.* Contact: Raymond J. Ho, Esq. Member (Partner)
Project: Product examination and chip analysis related to product infringement.
Represent:
Subject:
Status: Closed

Date: 2001 **Morgan Lewis & Bockius LLP**
Case: unknown
Project: Patent examination.
Represent:
Subject:
Status: Closed

Date: 1999-00 **Townsend Townsend & Crew**
Case *Sun Microsystems v. IBM.*
Parties: Sun Microsystem, IBM Corp.

	Project:	Patent infringement dispute related to computer circuits and logic: Study of patents and publications, preparation of expert report.
	Represent:	Sun Microsystem
	Subject:	Computer circuits and logic
	Status:	Case successfully settled
Date:	1998	**Weil Gotshal & Manges LLP**
	Case:	unknown
	Parties:	
	Project:	Patent examination. Two patents examined.
	Represent:	
	Subject:	
	Status:	Closed
Date:	1997-98	**Bernstein Litowitz Berger & Grossmann LLP**
	Case:	Edward McDaid, et al., On Behalf Of Themselves and All Others Similarly Situated v. Walter J. Sanders, III, et al., USDC, N.D. Cal., Case No. CV95-20750
	Parties:	Edward McDaid, et al., On Behalf Of Themselves and All Others Similarly Situated, Walter Jeremiah Sanders, III, Anthony B. Holbrook, Richard Previte, Marvin D. Burkett, Advanced Micro Devices, Inc.
	Project:	Class action case, analysis of AMD K5 processor design, *writing expert report* and participating in deposition as an assisting expert to the attorney.
	Represent:	Edward McDaid, et al.
	Subject:	Microprocessor design, AMD K5, schedule, debug, project management
	Status:	Case successfully settled (award amount $15 million)

Employment History:

From: 2018 **SambaNova Systems Inc.**
To: 2023 Palo Alto, California
Position: Senior Principal Engineer
Machine Learning: Processor design and development. Responsible for the Arithmetic Unit.

From: 2016 **Esperanto Technologies Inc**
To: 2018 Mt. View, California
Position: Founding Member
Massively parallel, ultra-low-power microprocessor system development. Working on low-power and low-voltage design in order to achieve minimal power operation for a given performance.

From: 2013 **Silicon Analytics Inc.**
To: 2020 San Jose, California
Position: Founder and President
Expertise and tool development for power optimization. Targeting low and ultra-low power design.

From: 2013 **Skyera Inc.**
To: 2014 San Jose, California
Position: *Senior Director, Processor Development*
Design of a massively parallel processor supporting Solid-State, Peta-Byte storage array. Managing entire processor design team.

From: 1996 **Integration Corp.**
To: Present Berkeley, California
Position: President and CEO
Processor design services: Developed fastest network encryption processor for Blue Steel Networks (sold to Broadcom for $150M). Designed and developed network encryption processor for Digital Archways. Design and developed Media and Floating-Point Processor for BOPS Inc.

From: 1992 **Advanced Computer Systems Engineering Laboratory**
To: Present Currently: Berkeley, California
Position: *Director*
Conducting research in: Low-Power systems and processor development with implementations in multi-media, cryptography and wireless communication. Developed a comprehensive family of clocked storage elements and clocking strategies for high performance and low-power applications; optimization method for digital circuits and system design resulting in up to 50% energy savings; the fastest parallel multiplier, adder and method for generation, estimation and comparison of arithmetic structures.

From: 1991 **University of California Davis**
To: Present Davis, CA

	Position:	Professor Emeritus, 2006-Present 1991-2006: Full Professor, Electrical and Computer Engineering Department
From:	2007	**University of Texas at Dallas**
To:	2010	Dallas, TX
	Position:	*Visiting Professor;* Director of Systems and Circuits Group (2007-2010), *Adjunct Professor (2010 – 2012)*
From:	2005	**Sydney University**
To:	2007	Sydney, Australia
	Position:	*Computer Engineering Chair and Chair Professor, Department of Electrical and Information Engineering* (ARC funding $1,900,000).
From:	03/2004	**Ecole Polytechnique Federale de Lausanne, EPFL**
To:	10/2004	Lausanne, Switzerland
	Position:	*Visiting Professor, Processor Architecture Laboratory* Developed and taught a new doctoral course in computer arithmetic
From:	07/2003	**Government of Korea**
To:	12/2003	Seoul, Korea
	Position:	*Distinguished Visiting Professor,* Korea Information Technology Assessment Program Established research program in digital media and secured a three year grant in *"Power Minimization for Media Signal Processing"* from the Korean government (appx: $300,000). Established and taught the course titled: *"Digital System Engineering"*.
From:	1998	**University of California at Berkeley**
To:	1990	Berkeley, CA
	Position:	*Visiting IBM Faculty, Electrical Engineering and Computer Science Department* **Teaching:** *Upper level courses:* CS150 Digital System Design, CS152: Computer System Design and Organization. *Graduate courses:* CS252 Computer System Architecture, CS292I VLSI Implementation of Fast Computer Arithmetic. Assisted in preliminary evaluation and preparation of Patterson-Hennessy book "Computer Architecture: A Quantitative Approach".
From:	1996	**Siemens Corporation**
To:	1998	San Jose, CA
	Position:	Architecture / Circuit Design Manager Development of Full-Custom high-performance arithmetic units. Chief architect for Siemens / Infineon TriCore line of integrated RISC-DSP controller. Development of and embedded Logic-DRAM processor (32-bit, RISC + DSP). Managed a group of 15 engineers.
From:	1982	**IBM T.J. Watson Research Center**
To:	1991	Yorktown Heights, NY

Position: *Research Staff Member*
My work was in the areas of: *Systems and Architecture, CPU and Floating-Point processor design, Circuit design, Design for Testability*
Development and implementation of VLSI RISC architectures:
1. High Performance 801 (first RISC microprocessor) for PC-RT (ROMP-E project).
2. Very high performance Super-Scalar RISC Architecture, RS/6000: floating point processor and system organization. (current PowerPC architecture)
3. Architectural definition and design of VLSI-RISC type processor to be used in a highly parallel super-computer. IBM SP-2.

From: 1979 **Xerox Corp.**
To: 1982 El Segundo, CA
Position: *Member of the Engineering Staff, Microelectronics Center*
Semiconductor wafer processing foundry of Xerox; automated the process parameter collection and designed a computer-controlled collection network; closely monitored process parameters and help point to faults and deviations to improve the wafer fabrication yield; managed process parameter collection and evaluation; designed an innovative process parameter testing structure, and worked in wafer testing.

From: 1977 **UCLA**
To: 1982 Los Angeles, CA
Position: *Research Assistant & Senior Research Engineer, Computer Science Department*
Worked on VLSI Design and Testability, VLSI Design Methodology, Fault-Tolerant Computer Design and High Reliability, Computer Arithmetic and Design of Arithmetic Processor.

From: 1974 **University of Belgrade**
To: 1976 Belgrade, Yugoslavia
Position: *Assistant Professor, Electrical Engineering Department*
Research and teaching in Analog and Digital Electronics.

From: 1973 **Institute for Automation and Telecommunications**
To: 1974 Belgrade Yugoslavia
Position: *Research Engineer*
Design of non-standard analog circuitry for the analog part of the state of the art hybrid computer (project with USSR). Design of an Analog Multiplier based on Time Division Concept.

From: 1971 **Institute of Physics**
To: 1973 Belgrade Yugoslavia
Position: *Research Physicist*
Experimental work in plasma physics with extensive use of computer tools for simulation and data acquisition. Written software in Fortran on IBM 360/44 and CDC 6600.

Consulting History Industry

From:	7/2016	**Esperanto Technologies, Inc.**
To:	4/2018	Mt View, California
	Duties:	processors
From:	10/2003	**Samsung Electronics Co. System LSI Division Research Laboratories**
To:	01/2004	Suwon-City, Gyeonggi-Do, Korea
	Duties:	Provided lectures on media processor architecture, clocking and clocked storage elements, power optimization of digital circuits.
From:	05/2002	**Intel Advanced Microprocessor Research Laboratories**
To:	09/2002	Hillsboro, OR
	Duties:	Developed Energy-Delay optimization methodology and tool for adders used in Itanium and P4 processors. Supervised two of my students in wireless 802.11 chip realization project.
From:	1997	**SONY, LSI Systems Laboratories**
To:	2001	San Jose, CA
	Duties:	Architect and project leader for new generation of media processors (reporting to the vice-president of SONY Corp.). Participated in strategic program planning as a member of the board.
From:	1996	**Hitachi Research and Development Laboratories**
To:	1999	San Jose, CA
	Duties:	Low-Power Design. Performed evaluation of clocked storage elements to be used in SH-5 processor. Work in low-power design.
From:	07/1994	**AT&T Bell Laboratories**
To:	09/1994	Holmdel, NJ
	Duties:	Development of new type of Low-Power circuits and logic based on energy-recovery principles.
From:	07/1992	**Sun Microsystems Laboratories**
To:	10/1992	Mountain View, CA
	Duties:	Worked on development of high-performance (1 GOP) super-scalar BiCMOS processor implementation and design.

PUBLICATIONS (Vojin G. Oklobdzija)

(Citations h-index = 46[4] ; 8,238 citations in Google Scholar; i10 index = 112)

BOOKS

[1] V. G. Oklobdzija, *"High-Performance System Design: Circuits and Logic,"* IEEE Press, July, 1999.

[2] V. G. Oklobdzija, *"Computer Engineering,"* CRC Press, December 2001. (Selected as "Outstanding Academic Title" in 2002 by Choice Magazine out of 22,000 titles).

[3] V. G. Oklobdzija et al, "Digital System Clocking: High-Performance and Low-Power Aspects," John Wiley Publishing, January 2003.

[4] V. G. Oklobdzija, R. K. Krishnamurthy, *"High Performance Energy Efficient Microprocessor Design,"* Springer, ISBN: 0-387-28594-6, June 2006.

[5] V. G. Oklobdzija, *"Digital Systems and Applications,"* Taylor & Francis Publishing, December 2007.

[6] V. G. Oklobdzija, *"Digital Design and Fabrication,"* Taylor & Francis Publishing, December 2007.

Books Published under my editorship in Computer Engineering book series:

[7] C. Piguet, "Low-Power Electronics Design," CRC Press, August, 2004.

[8] B. Vasic, E. M. Kurtas, "Coding and Signal Processing for Magnetic Recording Systems," CRC Press, November 2004.

[9] T. Reed, "Digital Image Sequence Processing, Compression and Analysis," CRC Press, 2004.

BOOK CHAPTERS:

[1] V. G. Oklobdzija, "Computer Arithmetic," The Electrical Engineering Handbook, R. C. Dorf (Ed.), a Chapter, CRC Press, Inc., pp. 1858-1865, 1993.

[2] V. G. Oklobdzija, "Computer Organization: Architecture," *The Engineering Handbook*, R. C. Dorf (Ed.), a Chapter, CRC Press, Inc., 1995.

[3] V. G. Oklobdzija, "Digital Systems" , *The Engineering Handbook*, R. C. Dorf (Ed.), Introduction into Digital Systems, Chapter, CRC Press, Inc., 1995.

[4] V. G. Oklobdzija, "Computers" , *The Engineering Handbook*, R. C. Dorf (Ed.), Introduction into Computers, a Chapter, CRC Press, Inc., 1995.

[4] **Wikipedia**: 45 or higher (h-index) could mean membership in the United States National Academy of Sciences. Hirsch estimated that after 20 years a "successful scientist" would have an *h*-index of 20, an "outstanding scientist" would have an *h*-index of 40, and a "truly unique" individual would have an *h*-index of 60.

[5] V. G. Oklobdzija, *"Digital Arithmetic,"* Wiley Encyclopedia of Electrical and Electronics Engineering, Book Chapter, John Wiley publishing, 1999.

[6] V. G. Oklobdzija, *"Reduced Instruction Set Computing,"* Vol.18, Wiley Encyclopedia of Electrical and Electronics Engineering, Book Chapter, John Wiley publishing, 1999.

[7] V. Oklobdzija, *"High-Speed VLSI Arithmetic Units: Adders and Multipliers,"* in "Design of High-Performance Microprocessor Circuits," Book Chapter, Book edited by A. Chandrakasan, IEEE Press, 2000.

[8] V. G. Oklobdzija, "Clocking Multi-GHz Systems," *Low-Power Electronics Design*, C. Piguet (Ed.), a Chapter, CRC Press, Inc., 2004.

[9] N. M. Nedovic, V. G. Oklobdzija, "Clocked Storage Elements in Digital Systems", in *"High Performance Energy Efficient Microprocessor Design"* V.G. Oklobdzija, R.K. Krishnamurthy (Ed.), a Chapter, Springer, 2006.

[10] V. G. Oklobdzija, B.R. Zeydel, "Design of Energy Efficient Digital Circuits", in *"High Performance Energy Efficient Microprocessor Design"* V.G. Oklobdzija, R.K. Krishnamurthy (Ed.), a Chapter, Springer, 2006.

[11] V. G. Oklobdzija, B.R. Zeydel, "Energy-Delay Charachteristics of CMOS Adders", in *"High Performance Energy Efficient Microprocessor Design"* V.G. Oklobdzija, R.K. Krishnamurthy (Ed.), a Chapter, Springer, 2006.

JOURNAL PAPERS:

[1] V. G. Oklobdzija and N. Konjevic, "Refractive-Ray Bending In Axially-Symmetric Plasma Sources," *Journal of Quantitative Spectroscopy and Radiative Transfer*, Vol. 14, pp. 389-394, 1974.

[2] V. G. Oklobdzija, "Up/Down Display Counter Counts Over Pos/Neg Range," *Digital Design*, pp. 94-95, 1981.

[3] V. G. Oklobdzija and M. D. Ercegovac, "An On-Line Square Root Algorithm," *IEEE Transactions on Computers*, Vol. C-31, No. 1, pp. 70-75, 1982.

[4] V. G. Oklobdzija, "Design Note. Opto-Isolated RS-232 Interface Achieves High Data Rate," Electronics, Vol. 55, No. 1, p. 175, 1982.

[5] V. G. Oklobdzija and E. R. Barnes, "Some Optimal Schemes For ALU Implementation In VLSI Technology," *Proceedings of the 7th Symposium on Computer Arithmetic ARITH-7*, pp. 2-8. Reprinted in *Computer Arithmetic*, E. E. Swartzlander, (editor), Vol. II, pp. 137-142, 1985.

[6] V. G. Oklobdzija and R. K. Montoye, "Design-Performance Trade-Offs In CMOS-Domino Logic," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 2, pp. 304-306, 1986.

[7] V. G. Oklobdzija and E. R. Barnes, "On Implementing Addition In VLSI Technology," *IEEE Journal of Parallel and Distributed Computing*, No. 5, pp. 716-728, 1988.

[8] B. D. Lee and V. G. Oklobdzija, "Improved CLA Scheme with Optimized Delay," *Journal of VLSI Signal Processing*, Vol. 3, No. 4, pp. 265-274, 1991.

[9] P. K. Chan, M. D. Schlag, C. D. Thomborson and V. G. Oklobdzija, "Delay Optimization of Carry-Skip Adders And Block Carry-Lookahead Adders Using Multidimensional Dynamic Programming," *IEEE Transaction on Computers*, Vol. 41, No. 8, pp. 920-930, 1992.

[10] V. G. Oklobdzija, "Algorithmic Design of A Hierarchical And Modular Leading Zero Detector Circuit," *Electronics Letters*, Vol. 29, No. 3, pp. 283-284, 1992.

[11] V. G. Oklobdzija, D. Villeger, and T. Soulas, "An Integrated Multiplier For Complex Numbers," *Journal of VLSI Signal Processing*, Vol. 7, No. 3, pp. 213-222, 1993.

[12] V. G. Oklobdzija, "An Algoritmic and Novel Design Of A Leading Zero Detector Circuit: Comparison With Logic Synthesis," *IEEE Transactions on VLSI Systems*, Vol. 2, No. 1, pp.124-128, 1993.

[13] D. Villeger and V. G. Oklobdzija, "Evaluation of Booth Encoding Techniques For Parallel Multiplier Implementation," *Electronics Letters*, Vol. 29, No. 23, pp. 2016-2017, 1993.

[14] V. G. Oklobdzija, "New ECL Gate in BiFET Process," *Electronics Letters*, Vol. 29, No. 23, pp. 2029-2030, 1993.

[15] V. G. Oklobdzija and D. Villeger, "Improving Multiplier Design By Using Improved Column Compression Tree And Optimized Final Adder In CMOS Technology," *IEEE Transactions on VLSI Systems*, Vol.3, No.2, June, 1995, 25 pages.

[16] M. N. Dorojevets and V. G. Oklobdzija, "Multithreaded Decoupled Architecture," *International Journal of High-Speed Computing*, World Scientific Publisher, 18 pages, June, 1995.

[17] K. J. Runge, P. Lee, J. Correa, R. T. Scalettar, and V. G. Oklobdzija, "Monte Carlo And Molecular Dynamics Simulations Using P4," Journal of High-Speed Computing, World Scientific Publisher, 27 pages, August 1995.

[18] V. G. Oklobdzija, "An ECL Gate with Improved Speed and Low Power in BiCMOS Process," Journal of Solid State Circuits, Vol.31, No.1, p.77-83, January 1996.

[19] V. G. Oklobdzija, D. Villeger, and S. S. Liu, "A Method for Speed Optimized Partial Product Reduction And Generation Of Fast Parallel Multipliers Using An Algorithmic Approach," *IEEE Transactions on Computers*, Vol.45, No.3, p. 294-306, March 1996.

[20] P. Stelling, V. G. Oklobdzija, "Design Strategies for Optimal Hybrid Final Adders in a Parallel Multiplier," special issue on VLSI Arithmetic, Journal of VLSI Signal Processing, Kluwer Academic Publishers, Vol.14, No.3, December 1996.

[21] R.H. Strandberg, J-C Le Duc, L.G. Bustamante, V. G. Oklobdzija, M. Soderstrand, "Efficient Realization of Squaring Circuit and Reciprocal used in Adaptive Sample Rate Notch Filters," special issue on VLSI Arithmetic, Journal of VLSI Signal Processing, Kluwer Academic Publishers, Vol.14, No.3, December 1996.

[22] V. G. Oklobdzija, "Comments on "Leading-Zero Anticipatory Logic for High-Speed Floating

Point Addition," IEEE Journal of Solid-State Circuits, Vol. 32, No. 2, pp.292-293, February 1997.

[23] W. Current, V. G. Oklobdzija, D. Maksimovic, "On Adiabatic Multiple Valued Logic Circuits," Journal of Multiple Value Logic, Vol.2, Gordon and Breach Publishing, pp.329-347, 1997.

[24] V. G. Oklobdzija, D. Maksimovic, F. C. Lin*, "Pass-Transistor Adiabatic Logic using Single Power-Clock Supply,"* IEEE Transactions on Circuits and Systems-II, Vol.44, No.10, pp.842-846. October 1997.

[25] V. G. Oklobdzija and B. Duchêne, *"Synthesis Of High-Speed Pass-Transistor Logic,"* IEEE Transactions on Circuits and Systems-II, Vol.44, No.11, November 1997, 7 pages.

[26] V. G. Oklobdzija, *"Differential and Pass-Transistor CMOS Logic for High-Performance Systems,"* reprinted from *21st International IEEE Conference on Microelectronics*, Electronics, Vol. 1, No. 1, December 1997.

[27] P. Stelling, C. Martel, V. G. Oklobdzija, R. Ravi, "Optimal Circuits for Parallel Multipliers," IEEE Transaction on Computers, Vol. 47, No.3, pp. 273-285, March, 1998.

[28] V. G. Oklobdzija, *"Differential and Pass-Transistor CMOS Logic for High-Performance Systems,"* Microelectronics Journal, Elsevier Publishing, Vol. 29, p.679-688, Spring 1998.

[29] V.Stojanovic and V.G. Oklobdzija, *"Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power VLSI Systems,"* IEEE Journal of Solid-State Circuits, Vol.34, No.4, April 1999.

[30] D. Markovic, B. Nikolic, V.G. Oklobdzija, *"General Method in Synthesis of Pass-Transistor Circuits,"* Microelectronics Journal, Elsevier Science Publishing, No. 31, November-December 2000, p.991-998.

[31] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, W. Jia, J. Chiu, M. Leung, *"Improved Sense Amplifier-Based Flip-Flop: Design and Measurements,"* IEEE Journal of Solid-State Circuits, Vol. 35, No. 6, June 2000.

[32] D. Maksimovic, V. G. Oklobdzija, B. Nikolic, K. W. Current, "*Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply*," IEEE Transactions on VLSI Systems, Vol.8, No.4, August 2000.

[33] Oklobdzija V. G. "*Clocking in multi-GHz environment*". Facta Universitatis, Nis, Electrical

Engineering Series, Vol.15, No.1. April 2002. (reprint from *23rd International Conference on Microelectronics. Proceedings, 2002*).

[34] V. G. Oklobdzija, *"Clocking and Clocked Storage Elements in Multi-GHz Environment,"* invited paper, IBM Journal of Research and Development, Vol. 47, No. 5/6, pp. 567-584, September/November 2003.

[35] N. Nedovic, W. Walker, V. G. Oklobdzija, *"A Test Circuit for Measurement of Clocked Storage Element Characteristics,"* IEEE Journal of Solid-State Circuits, Vol.29, No.8, August 2004.

[36] N. Nedović, V. G. Oklobdzija, "Dual-Edge Triggered Storage Elements and Clocking Strategy for Low-Power Systems," *IEEE Transaction on VLSI Systems*, Volume 13, Issue 5, pp. 577-590, May 2005.

[37] V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, R. Krishnamurthy, "Comparison of High- Performance VLSI Adders in Energy-Delay Space," *IEEE Transaction on VLSI Systems*, Volume 13, Issue 6, pp. 754-758, June 2005.

[38] S. K. Hsu, S. K. Mathew, M. A. Anders, B. R. Zeydel, V. G. Oklobdzija, R. K. Krishnamurthy, S.Y. Borkar, *"A 110 GOPS/W 16-bit Multiplier and Reconfigurable PLA Loop in 90-nm CMOS,"* IEEE Journal of Solid-State Circuits, Vol.41, No.1, January 2006.

[39] H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, *"Energy Optimization of Pipelined Digital Systems Using Circuit Sizing and Supply Scaling,"* IEEE Transaction on VLSI Systems, Vol.14, No.2, February, 2006.

[40] N. Nedovic, C. Giacomotto, V. G. Oklobdzija, *"The Effect of System Specification to the Optimal Choice of Clocked Storage Element,"* IEEE Journal of Solid-State Circuits, June 2007.

[41] M. Aleksic, K. W. Current, V. G. Oklobdzija, "Jitter Analysis of Non-Autonomous MOS Current-Mode Logic Circuits" *IEEE Transaction on Circuits and Systems I, Special Issue, Vol. 55, No.10, November 2008.*

[42] H. Karimiyan Alidash and V. G. Oklobdzija., "Low-Power Soft Error Hardened Latch," *Journal Low Power Electronics 6, 218-226* (2010).

[43] B. R. Zeydel, D. Baran, V. G. Oklobdzija, *"Energy Efficient Design of High-Performance VLSI Adders"*, IEEE Journal of Solid-State Circuits, Vol.45, No.6, June 2010.

CONFERENCE PROCEEDINGS:

[1] V. Oklobdzija and N. Konjevic, "Spectroscopy of Axisymmetric Plasma Sources," *Proceedings of the Eleventh International Conference on Phenomena in Ionized Gases*, p. 449, 1973.

[2] V. G. Oklobdzija and N. Konjevic, "Refractive-Ray Bending In Axially-Symmetric Plasma Sources," Proceedings of the International Conference on the Physics of Ionized Gases, 1974.

[3] V. G. Oklobdzija and M. D. Ercegovac, "Testability Enhancement of VLSI Using Circuit Structures," *Proceedings of IEEE International Conference on Circuits and Computers*, ICCC '82, pp. 198-201, 1982.

[4] V. G. Oklobdzija, "Improving Testability by Using Additional Circuits," *Proceedings of the Seventeenth Asilomar Conference on Circuits, Systems and Computers*, pp. 118-123, 1983.

[5] J. P. Roth, V. G. Oklobdzija and J. F. Beetem, "Test Generation for FET Switching Circuits," *Proceedings of the International Test Conference*, pp. 59-62, 1984.

[6] V. G. Oklobdzija and P. G. Kovijanic, "On Testability Of CMOS-Domino Logic," Proceedings *FTCS-14: 14th IEEE International Conference on Fault- Tolerant Computing*, pp. 50-55, 1984.

[7] V. G. Oklobdzija and R. K. Montoye, "Design-Performance Trade-Offs in CMOS Domino Logic," *Proceedings of the Custom Integrated Circuits Conference*, pp. 334-337, 1985.

[8] V. G. Oklobdzija, N. M. Marinovic and L. Roytman, "Single-Chip Architecture for Real-Time Computation Of The Wigner Distribution Of Acoustic Signals," *Proceedings of the 21st Asilomar Conference on Signals, Systems and Computers*, pp. 939-943, 1987.

[9] V. G. Oklobdzija, "Architecture for Single-Chip ASIC Processor With Integrated Floating Point Unit," *Proceedings of the 21st Hawaii International Conference on System Sciences*, pp. 1-9, 1988. (Best Paper award)

[10] N. M. Marinovic, V. G. Oklobdzija and L. Roytman, "VLSI Architecture of A Real-Time Wigner Distribution Processor For Acoustic Signals," *Proceedings of the International Conference on Acoustics, Speech, and Signal Processing*, V4.7, pp. 2112-2115, 1988.

[11] V. G. Oklobdzija and G. Grohosky, "Architectural Study for An Integrated Fixed And Floating-Point VLSI-ASIC Processor," COMPEURO-'88, *IEEE Symposium on Circuits and Systems*, pp. 108-115, 1988.

[12] V. G. Oklobdzija, “Simple and Efficient CMOS Circuit for Fast VLSI Adder Realization,” *Proceedings of the International Symposium on Circuits and Systems*, pp. 1-4, 1988.

[13] V. G. Oklobdzija, “Issues In CPU-Coprocessor Communication and Synchronization,” EUROMICRO '88, *Fourteenth Symposium, Microprocessing and Microprogramming*, North-Holland Publishers, Vol. 24, pp. 695-700, 1988.

[14] V. G. Oklobdzija, “Rapid Turn-Around Design Style and Technology: Impact on Computer Architecture,” *Proceedings of the 22nd Annual Hawaii International Conference on System Sciences* (HICSS-22), Vol. 1, page 1, 1989.

[15] B. D. Lee and V. G. Oklobdzija, “Optimization and Speed Improvement Analysis of Carry- Lookahead Adder Structure,” *Proceedings of the 24th Asilomar Conference on Signals, Systems and Computers*, Vol. 2 of 2, pp. 918-922, 1990.

[16] P. K. Chan, M. D. F. Schlag, C. D. Thomborson and V. G. Oklobdzija, “Delay Optimization of Carry-Skip Adders and Block Carry-Lookahead Adders,” *Proceedings of the 10th IEEE Symposium on Computer Arithmetic* ARITH-10, pp. 1-11, 1991.

[17] A. Sah, D. C. Verma and V. G. Oklobdzija, A Study Of I/O Architecture for High Performance Next Generation Computers,” *Proceedings of the 2nd Symposium on High*

Performance Computing, pp. 1-12, 1991.

[18] N. M. Marinovic and V. G. Oklobdzija, “VLSI Chip Architecture for Real-Time Ambiguity Function Computation,” *Proceedings of the 25th Asilomar Conference on Signals, Systems and Computers*, 1991, 5 pages.

[19] V. G. Oklobdzija, “An Implementation Algorithm and Design Of A Novel Leading Zero Detector Circuit,” *26th IEEE Asilomar Conference on Signals, Systems and Computers*, Vol.1, pp. 391-395, 1992. (Invited paper)

[20] V. G. Oklobdzija, D. Villeger, and T. Soulas, “Considerations for Design Of A Complex Multiplier,” *26th IEEE Asilomar Conference on Signals, Systems and Computers, Asilomar*, Vol. 1, pp. 366-370, 1992. (Invited paper)

[21] T. Soulas, D. Villeger and V. G. Oklobdzija, “An ASIC Macro Cell Multiplier for Complex Numbers,” *Proceedings of EURO-ASIC-93, the European (EDAC) Conference in ASIC Design*, 1993. 5 pages.

[22] V. G. Oklobdzija and D. Villeger, “Multiplier Design Utilizing Improved Column Compression Tree and Optimized Final Adder In CMOS Technology,” *Proceedings of the 1993 International Symposium on VLSI Technology, Systems and Applications*, pp. 209-212, 1993.

[23] V. G. Oklobdzija, “A Hierarchical and Modular Circuit Implementing Leading Zero Detector For A High-Performance Floating-Point Processor,” *Proceedings of the 5th International Symposium on IC Technology, Systems, and Applications*, ISIC-93, Nanyang Technological University, Singapore, 1993, 2 pages.

[24] D. Villeger and V. G. Oklobdzija, "Analysis of Booth Encoding Efficiency in Parallel Multipliers Using Compressors for Reduction Of Partial Products," *Proceedings of the 27th Asilomar Conference on Signals, Systems and Computers*, pp. 781-784, 1993.

[25] M. Q. Le and V. G. Oklobdzija, "Logic Synthesis For ASIC: A Guided Algorithmic Approach," *Proceedings of the 1994 International Conference on ASIC*, 1994, 4 pages.

[26] A. de la Serna, M. A. Soderstrand and V. G. Oklobdzija, "System for Rapid Prototyping of Application Specific Signal Processors for ASIC Implementation," *Proceedings of the 1994 International Conference on ASIC Implementation*, pp. 157-160, 1994.

[27] R. Hundal and V. G. Oklobdzija, "Determination of Optimal Sizes for A First and Second Level SRAM-DRAM On-Chip Cache Combination," *Proceedings of the 1994 International Conference on Computer Design*, 1994, 5 pages.

[28] V. G. Oklobdzija, "An ECL Gate with Improved Speed and Low Power in BiCMOS Process," *Proceedings of the 1994 Bipolar/BiCMOS Circuits and Technology Meeting*, 1994, 4 pages.

[29] V. G. Oklobdzija, "Design and Analysis of Fast Carry-Propagate Adder Under Non-Equal Input Signal Arrival Profile," *Proceedings of the 28th Asilomar Conference on Signals, Systems and Computers*, 1994, 4 pages.

[30] R. H. Strandberg, J. C. Le Duc, Z-Y. Yang, L. G. Bustamante, V. G. Oklobdzija and M. Soderstrand, "Reconfigurable Processor For Real-Time Adaptive Sample Rate Notch Filtering," *Proceedings of the 28th Asilomar Conference on Signals, Systems and Computers*, 1994, 4 pages.

[31] R. H. Strandberg, J. C. Le Duc, L. G. Bustamante, V. G. Oklobdzija, and M. Soderstrand, "Implementation of Adaptive Sample Rate Kwan-Martin Notch Filter Using Efficient Realizations of Reciprocal And Squaring," *Proceedings of the 28th Asilomar Conference on Signals, Systems and Computers*, 1994, 5 pages.

[32] K. J. Runge, P. Lee, J. Correa, R.T. Scalettar, V.G. Oklobdzija, "Monte Carlo and Molecular Dynamic Simulations Using P4," *Proceedings of the 9th Int'l Parallel Processing Symposium*, Santa Barbara, California, 7 pages, April 24-29, 1995.

[33] D. Maksimovic, V.G. Oklobdzija, "Integrated Power Clock Generators for Low Energy Logic*," Proceedings of the 1995 Power Electronics Specialists Conference*, Atlanta, Georgia, June 18-22, 1995.

[34] V. G. Oklobdzija and B. Duchêne, "Pass-Transistor Dual Value Logic for Low-Power CMOS*," Proceedings of the 1995 International Symposium on VLSI Technology*, Taipei, Taiwan, May 31-June 2nd, 1995.

[35] C. Martel, V. G. Oklobdzija, R. Ravi and P. Stelling, "Design Strategies for Optimal Multiplier Circuits," *Proceedings of the 12th IEEE Symposium on Computer Arithmetic*, Bath, ENGLAND, July 19-21,1995, 19 pages.

[36] V. G. Oklobdzija and B. Duchêne, "Logic Synthesis for Pass-Transistor Design," *IEEE International Conference on Solid-State and Integrated-Circuit Technology*, October 24-28, 1995, Beijing, China.

[37] V. G. Oklobdzija and B. Duchêne, "Pass-Transistor Logic Family for High-Speed and Low-Power CMOS," *Sixth International Symposium on IC Technology, Systems and Applications*, ISIC-95, Singapore, September 6-8, 1995.

[38] D. Maksimovic, V. G. Oklobdzija, "Clocked CMOS Adiabatic Logic with Single AC Power Supply," 21st *European Solid-State Circuits Conference*, September 19-21, 1995, Lille, FRANCE.

[39] V. G. Oklobdzija and B. Duchêne, "Development and Synthesis Method for Pass-Transistor Logic Family for High-Speed and Low Power CMOS," 38*th Midwest Symposium on Circuits and Systems*, Rio de Janeiro, BRASIL, August 13-16, 1995.

[40] P. Bonatto, V. G. Oklobdzija, "Evaluation of Booth's Algorithm for Implementation in Parallel Multipliers," *Twenty-Ninth Annual Asilomar Conference on signals, Systems and Computers*, Pacific Grove, California, October 29 - November 1, 1995.

[41] Jean Noel, V. G. Oklobdzija, "New Pipelined Architecture for DSP," *Twenty-Ninth Annual Asilomar Conference on signals, Systems and Computers*, Pacific Grove, California, October 29 - November 1, 1995.

[42] V. G. Oklobdzija, P. Stelling "Design Strategies for the Final Adder in a Parallel Multiplier," *Twenty-Ninth Annual Asilomar Conference on signals, Systems and Computers*, Pacific Grove, California, October 29 - November 1, 1995.

[43] V. G. Oklobdzija, "A Method for Generation of Fast Parallel Multipliers," *2nd International Conference on Massively Parallel Computing Systems*, May 6-9, 1996, Ischia, ITALY.

[44] W. Current, V. G. Oklobdzija, D. Maksimovic, "Low-Energy Logic Circuit Techniques for Multiple-Value Logic," *Second Int'l Symposium on Multiple-Valued Logic*, Santiago de Compostela, Spain, May 29-31, 1996.

[45] P. Stelling, V. G. Oklobdzija, "Implementing Multiply-Accumulate Operation in the Multiply Time," *Thirteenth International Symposium on Computer Arithmetic*, Pacific Grove, California, July 5 - 9, 1997.

[46] D. Maksimovic, V. G. Oklobdzija, B. Nikolic, K. Wayne Current, *"Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply: Experimental Results,"* International Symposium on Low Power Electronics and Design, August 18-20, 1997, Monterey, California.

[47] D. Maksimivic, V. G. Oklobdzija, B. Nikolic, K. Wayne Current, "Design and Experimental Verification of a CMOS Adiabatic Logic with Single-Phase Power-Clock Supply," Proceedings of the 40th Midwest Symposium on Circuits and Systems, August 3-6, 1997, Sacramento, California.

[48] Paul F. Stelling and Vojin G. Oklobdzija*, "Optimal Designs for Multipliers and Multiply-Accumulators,"* Proceedings of the 15th IMACS World Congress on Scientific Computation, Modeling, and Applied Mathematics, Volume 4 Artificial Intelligence and Computer Science, Achim Sydow, editor, Wissenschaft and Technik Verlag, Berlin, August 1997, pp. 739-744.

[49] B. Nikolic, V. G. Oklobdzija, “A Single-Phase Clock High-Performance BiCMOS Latch*,” Proceedings of the 7th International Symposium on IC Technology, Systems & Applications,* September 10-12, 1997, Singapore.

[50] V. G. Oklobdzija, “Differential and Pass-Transistor CMOS Logic for High-Performance Systems,” *21st International IEEE Conference on Microelectronics*, September 15-17, 1997, Nis, Yugoslavia.

[51] P. Stelling, C. Martel, V. G. Oklobdzija, R. Ravi, “Optimal Circuits for Parallel Multipliers,” IEEE Transaction on Computers, Vol. 47, No.3, pp. 273-285, March 1998.

[52] A. Farooqui, V. G. Oklobdzija, *“General Data-Path Organization of a MAC unit for VLSI Implementation of DSP Processors,”* IEEE International Symposium on Circuits and Systems, Monterey, California, May 31 - June 3, 1998.

[53] B. Nikolic, V. G. Oklobdzija, " Low Voltage BiCMOS TSPC Latch for High Performance Digital System,” IEEE International Symposium on Circuits and Systems, May 31 - June 3, 1998, Monterey, California.

[54] V. G. Oklobdzija, “Architectural Tradeoffs for Low Power,” International Symposium on Computer Architecture, Barcelona, SPAIN, June 27-July 1st, 1998.

[55] V. Stojanovic, V. G. Oklobdzija, R. Bajwa, *“A Unified Approach in the Analysis of Latches and Flip-Flops for Low-Power,”* International Symposium on Low Power Electronics and Design, August 10-12, 1998, Monterey, California.

[56] V. Stojanovic, V. G. Oklobdzija, R. Bajwa, *“Comparative analysis of Master-Slave Latches and Flip-Flops for HIgh-Performance VLSI Systems,”* International Conference on Computer Design, October 5-7, 1998, Austin, Texas.

[57] A. A. Farooqui, V. G. Oklobdzija, "Early Branch Prediction circuit for application in DSP,” 1998 IEEE Conference on Microelectronics, Monastir, Tunisia, December 14-16, 1998.

[58] B. Nikolic, V. Stojanovic, V.G. Oklobdzija, W. Jia, J. Chiu, M. Leung, "Sense Amplifier Based Flip-flop," to be presented at 1999. IEEE International Solid-State Circuits Conference, San Francisco, February 1999.

[59] A. Farooqui, V. G. Oklobdzija, *"VLSI implementation of early branch prediction circuits,”*

9th Great Lakes VLSI conference (GLSVLSI 99), Ann Arbor, Michigan, March 4-6, 1999.

[60] A. Farooqui, V. G. Oklobdzija, F. Chehrazi, *"64-Bit Media Adder,”* 1999 IEEE International Symposium on Circuits and Systems, Orlando, Florida, May 5-8, 1999.

[61] A. Farooqui, V. G. Oklobdzija, F. Chehrazi, *"Multiplexer Based Adder for Media Signal Processing,”* 1999 International Symposium on VLSI Technology, Systems, and Applications, Taipei, Taiwan, June 8-10, 1999.

[62] B. Nikolic, M. Leung, L. Fu, V.G. Oklobdzija, R. Yamasaki, Reduced-Complexity Sequence Detection for EEPR4 Magnetic Recording Channel, " 1999. International Conference on Communications, Vancouver, June 1999.

[63] D. Markovic, B. Nikolic, V.G. Oklobdzija, "General Method in Synthesis of Pass-Transistor Circuits" *22nd International IEEE Conference on Microelectronics*, May, 2000, Nis, Yugoslavia.

[64] V. G. Oklobdzija, A. A. Farooqui, *"Computer Arithmetic for the Processing of Media Signals,"* Invited Paper, Proceedings of SPIE Vol. 4116, Advanced Signal Processing Algorithms, Architectures, and Implementations, San Diego, California, USA, 2 -4 August 2000.

[65] A. Farooqui, K. W. Current, V. G. Oklobdzija, *"Partitioned Branch Condition Resolution Logic,"* Proceedings of the Symposium on Integrated Circuits and Systems Design, SBCCI2000, Manaus, Brazil, September 18-22, 2000.

[66] N. Nedovic, V. G. Oklobdzija, *"Hybrid Latch Flip-Flop with Improved Power Efficiency,"* Proceedings of the Symposium on Integrated Circuits and Systems Design, SBCCI2000, Manaus, Brazil, September 18-22, 2000.

[67] N. Nedovic, V. G. Oklobdzija, *"*Dynamic Flip-Flop with Improved Power," Proceedings of the 26th European Solid-State Circuits Conference, ESSCIRC'2000, Stockholm, Sweden, September 19-21, 2000.

[68] N. Nedovic, V. G. Oklobdzija, *"*Dynamic Flip-Flop with Improved Power," Proceedings of the International Conference on Computer Design, ICCD 2000, Austin, Texas, September 18-20, 2000.

[69] A Farooqui, V. G. Oklobdzija, *"Impact of Architecture Extensions for Media Signal Processing on Data-Path Organization,"* 34th Annual Asilomar Conference on signals, Systems and Computers, Pacific Grove, California, October 29 - November 1, 2000.

[70] A. A Farooqui, V. G. Oklobdzija, *"A Programmable Data-Path for MPEG-4 and Natural Hybrid Video Coding,"* 34th Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, California, October 29 - November 1, 2000.

[71] V. G. Oklobdzija, "Computer Arithmetic for Processing of Media Signals," 34th Annual Asilomar Conference on signals, Systems and Computers, Pacific Grove, California, October 29 - November 1, 2000.

[72] D. Markovic, B. Nikolic, V.G. Oklobdzija, *"General Method in Synthesis of Pass-Transistor Circuits,"* Microelectronics Journal, Elsevier Science Publishing, No. 31, November-December 2000, p.991-998.

[73] A. Inoue, V. G. Oklobdzija, W. W. Walker, M. Kai, T. Izawa, *"A Low Power SOI Adder Using Reduced-Swing Charge Recycling Circuits,"* 2001 IEEE International Solid-State Circuits Conference Digest of Technical papers, San Francisco, February 2001.

[74] Nedovic Nikola; Oklobdzija, Vojin G.; Leung, Michael (USA): "FIR Filter for Adaptive Equalization in PRML Read Channels," The 5th World Multi-Conference on Systemics, Cybernetics and Informatics SCI 2001, Orlando, Florida, July 22-25, 2001.

[75] Hoang Dao, Kevin Nowka, Vojin G. Oklobdzija, *"Analysis of Clocked timing Elements for DVS Effects over Process Parameter Variations,"* Proceedings of the International

Symposium on Low Power Electronics and Design, Huntington Beach, California, August 6-7, 2001.

[76] Nikola Nedovic, Marko Aleksic and Vojin G. Oklobdzija, *"Conditional Techniques for Small Power Consumption Flip-Flops,"* Proceedings of the 8th IEEE International Conference on Electronics, Circuits and Systems, Malta, September 2-5, 2001.

[77] Nikola Nedovic, Marko Aleksic and Vojin G. Oklobdzija, *"Timing Characterization of Dual-Edge Triggered Flip-Flops,"* Proceedings of the International Conference on Computer Design, ICCD 2001, Austin, Texas, September 23-26, 2001.

[78] Hoang Q. Dao, Vojin G. Oklobdzija, *"Application of Logical Effort on Delay Analysis of 64-bit Static Carry-Lookahead Adder,"* 35th Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, California, November 4-7, 2001.

[79] Xiao Yan Yu, Vojin G. Oklobdzija, William W. Walker, *"Application of Logical on Design of Arithmetic Blocks,"* 35th Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, California, November 4-7, 2001.

[80] Hoang Q. Dao, Vojin G. Oklobdzija, *"Application of Logical Effort Techniques for Speed Optimization and Analysis of Representative Adders,"* 35th Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, California, November 4-7, 2001.

[81] Martin Saint-Laurent, Vojin G. Oklobdzija, Simon S. Singh, Madhavan Swaminathan, and James D. Meindl, *"Optimal Synchronization Energy Allocation for CMOS Integrated Systems,"* 3rd International Symposium on Quality Electronic Design, March 18-20, 2002, San Jose, California, USA.

[82] Nikola Nedovic, Marko Aleksic, Vojin G. Oklobdzija, *"Comparative Analysis of Double-Edge versus Single-Edge Triggered Clocked Storage Elements,"* 2002 IEEE International Symposium on Circuits and Systems, Scottsdale, Arizona, May 26-29, 2002.

[83] Aamir A. Farooqui, Vojin G. Oklobdzija, "Placement and Area-Time Driven Optimal AdderDesign," International Symposium on Optical Science and Technology, July 7-11, 2002.

[84] Nikola Nedovic, Marko Aleksic, Vojin G. Oklobdzija, *"Conditional Pre-Charge Techniques for Power-Efficient Dual-Edge Clocking,"* Proceedings of the International Symposium on Low-Power Electronics and Design, Monterey, California, August 12-14, 2002.

[85] Oklobdzija VG, Sparso J. "*Future directions in clocking multi-GHz systems*". ISLPED'02: Proceedings of the 2002 International Symposium on Lower Power Electronics and Design (IEEE Cat. No.02TH8643). ACM. 2002, pp.219. New York, NY, USA.

[86] Hoang Dao, Vojin G. Oklobdzija, "Performance Comparison of VLSI Adders Using Logical Effort," 12th International Workshop on Power and Timing Modeling, Optimization and Simulation, Sevilla, SPAIN, September 11-13, 2002. *Proceedings (Lecture Notes in Computer Science Vol.2451). Springer-Verlag. 2002, pp.25-34. Berlin, Germany.*

[87] Vojin G. Oklobdzija, "Clocking and Clocked Storage Elements in Multi-GHz Environment," Invited paper, 12th International Workshop on Power and Timing Modeling, Optimization and Simulation, Sevilla, SPAIN, September 11-13, 2002. *Proceedings (Lecture Notes in Computer Science Vol.2451). Springer-Verlag. 2002, pp.128-45. Berlin, Germany.*

[88] Nikola Nedovic, William W. Walker, Vojin G. Oklobdzija, Marko Aleksic, *"A Low Power Symmetrically Pulsed Dual Edge-Triggered Flip-Flop,"* Proceedings of the 28th European Solid-State Circuits Conference, Florence, ITALY, September 24-26, 2002.

[89] N. Nedovic, V. G. Oklobdzija, W. W. Walker, *"A Clock Skew Absorbing Flip-Flop,"* 2003 IEEE International Solid-State Circuits Conference Digest of Technical papers, San Francisco, February 2003.

[90] Aamir A. Farooqui, Vojin G. Oklobdzija, Sadiq M. Sait, "*Area-Time Optimal Adder with Relative Placement Generator,"* International Symposium on Circuits and Systems, May 25-28, 2003, Bangkok, Thailand, 2003.

[91] Xiao Yan Yu, Vojin G. Oklobdzija, William W. Walker, "An Efficient Transistor Optimizer for Custom Circuits," International Symposium on Circuits and Systems, May 25-28, 2003, Bangkok, Thailand, 2003.

[92] B.R. Zeydel, V.G. Oklobdzija, S. Mathew, R.K. Krishnamurthy, S. Borkar, "*A 90nm 1GHz 22mW 16x16-bit 2's Complement Multiplier for Wireless Baseband*," Proceedings of the 2003 Symposium on VLSI Circuits, Kyoto, JAPAN, June 12 - 14, 2003.

[93] Vojin G. Oklobdzija, Bart R. Zeydel, Hoang Dao, Sanu Mathew, Ram Krishnamurthy, "*Energy-Delay Estimation Technique for High-Performance Microprocessor VLSI Adders*," Proceedings of the International Symposium on Computer Arithmetic, ARITH-16, Santiago de Compostela, SPAIN, June 15-18, 2003.

[94] Hoang Q. Dao, Bart R. Zeydel, Vojin G. Oklobdzija, "*Energy Minimization Method for Optimal Energy-Delay Extraction*," Proceedings of the European Solid-State Circuits Conference, ESSCIRC 2003, Estoril, PORTUGAL, September 16-18, 2003.

[95] Hoang Q. Dao, Bart R. Zeydel, Vojin G. Oklobdzija, *"Energy Optimization of High-Performance Circuits,"* Proceedings of the 13th International Workshop on Power and Timing Modeling, Optimization and Simulation, Torino, ITALY, September 10-12, 2003.

[96] Vojin G. Oklobdzija, *"Multi GHz Systems Clocking,"* Invited Paper, Proceedings of the 5th International Conference on ASIC, Beijing, P.R. China, October 22-24, 2003.

[97] Vojin G. Oklobdzija, *"Issues in System on the Chip Clocking,"* Invited Paper, Proceedings of the IEEK System on Chip Design Conference, Seoul, Korea, November 5-6, 2003.

[98] Milena Vratonjic, Bart R. Zeydel, Hoang Q. Dao, Vojin G. Oklobdzija, *"Low-Power Aspects of Different Adder Topologies,"* 37th Annual Asilomar Conference on Signals, Systems and Computers, Pacific Grove, California, November 9-12, 2003.

[99] Hoang Q. Dao, Bart R. Zeydel, Victor Zyuban, and Vojin G. Oklobdzija, "On Energy Optimization of Digital Systems," The fourth annual IBM Austin Conference on Energy-Efficient

Design, ACEED 2005, Austin, Texas, March 1-3, 2005.

[100] Bart R. Zeydel, Theo T.J.H. Kluter, Vojin G. Oklobdzija, "*Efficient Mapping of Addition Recurrence Algorithms in CMOS*," Proceedings of the International Symposium on Computer Arithmetic, ARITH-17, Cape Cod, Massachusetts, June 27-29, 2005.

[101] M. Aleksić, N. Nedović, K. W. Current, V. G. Oklobdzija, "A New Model for Timing Jitter Caused by Device Noise in Current-Mode Logic Frequency Dividers," *in Proc. of the 15th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Leuven, Belgium, September 21-23, 2005*.

[102] H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Architectural Considerations for Energy Efficiency: Case Study of Viterbi Decoder ACS Unit," *Proceedings of the International Conference on Computer Design, ICCD 2005, San Jose, California, October 2-5, 2005.*

[103] M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija, "Low- and Ultra Low-Power Arithmetic Units: Design and Comparison ," *Proceedings of the International Conference on Computer Design, ICCD 2005, San Jose, California, October 2-5, 2005.*

[104] H. Q. Dao, B. R. Zeydel, V. G. Oklobdzija, "Energy-Efficient Optimization of the Viterbi ACS Unit Architecture," *Proceedings of the Asian Solid-State Circuit Conference, A-SSCC 2005, Hsinchu, Taiwan, November 1-3, 2005*.

[105] Christophe Giacomotto, Nikola Nedovic, Vojin G. Oklobdzija, "Energy-Delay Space Analysis and Clocked Storage Elements under Process Variability," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2006*, Montpelier, FRANCE.

[106] Xiao Yan Yu1,4, Robert Montoye2, Kevin Nowka3, Bart Zeydel4 and Vojin Oklobdzija4 , "Estimating Energy Efficiency: Comparing LSDL and Compound Domino," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2006*, Montpelier, FRANCE.

[107] Milena Vratonjic, Bart R. Zeydel, Vojin G. Oklobdzija, "Circuit Sizing and Supply-Voltage Selection Effects in Low-Power Design," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2006*, Montpelier, FRANCE.

[108] Bart R. Zeydel and Vojin G. Oklobdzija, "Methodology for Energy-Efficient Digital Circuit Sizing: Important Issues and Design Limitations," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2006*, Montpelier, FRANCE.

[109] Mandeep Singh, Christophe Giacomotto, Bart R. Zeydel and Vojin G. Oklobdzija, "Logic Style Comparison for Ultra Low-Power Operation in 65nm Technology," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2007*, Goeteborg, SWEDEN.

[110] Christophe Giacomotto , Mandeep Singh, Milena Vratonjic, Vojin G. Oklobdzija, "Energy Efficiency of Power-Gating in Low-Power Clocked Storage Elements," *Power and Timing Modeling, Optimization and Simulation, PATMOS 2008*, Lisbon, PORTUGAL.

[111] D. Baran, M. Aktan, H. Karimiyan, V. G. Oklobdzija, "Exploration of Switching Activity Behavior of Addition Algorithms", *IEEE MWSCAS 2009*, Cancun, Mexico, 2-5 August 2009.

[112] Joosik Moon, Mustafa Aktan, V. G. Oklobdzija, "Design Methodology for Clocked Storage Elements Robust to Process Variations", CENICS 2009, Sliema, Malta, 11-16 October 2009.

[113] D. Baran, M. Aktan,H. Karimiyan, V. G. Oklobdzija, "Switching Activity Calculation of VLSI Adders", the IEEE ASICON 2009, Changsha, China, 20-23 October 2009.

[114] Joosik Moon, Mustafa Aktan, V. G. Oklobdzija, "Clocked Storage Elements Robust to Process Variations", the IEEE ASICON 2009, Changsha, China, 20-23 October 2009.

[115] H. K. Alidash, S. M. Sayedi, H. Saidi, and V. G. Oklobdzija, "Soft Error Filtered and Hardened Latch," the IEEE ASICON2009, Changsha, China, 20-23 October 2009.

[116] M. Aktan, S. Paramesvaran, J. Moon, and V. G. Oklobdzija, "Energy-Delay Space Exploration of Clocked Storage Elements Using Circuit Sizing," the Austin conference on Integrated systems and Circuits (ACISC), Austin, 2009.

[117] H. K. Alidash and V. G. Oklobdzija, "Low-Power Soft Error Hardened Latch," PATMOS 2009, 19th international Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Delft, Holland, 2009.

[118] M. Vratonjic, M. Ziegler, G. D. Gristede, V. Zyuban, T. Mitchell, E. Cho, C. Visweswariah, V. G. Oklobdzija, "A New Methodology for Power-Aware Transistor Sizing: Free Power Recovery (FPR)", PATMOS 2009, 19th international Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), Delft, Holland, 2009.

[119] Baran, Dursun; Aktan, Mustafa; Oklobdzija, Vojin G.; , " Energy efficient implementation of parallel CMOS multipliers with improved compressors," *2010 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)* , pp.147-152, 18-20 Aug. 2010.

[120] Baran, Dursun; Aktan, Mustafa; Oklobdzija, Vojin G.; , " Multiplier Structures for Low Power Applications in Deep-CMOS," *Proceedings of 2011 IEEE International Symposium on Circuits and Systems (ISCAS)* , pp., 15-18 May. 2011.

[121] Aktan, Mustafa; Baran, Dursun; Oklobdzija, Vojin G.; "A Quick Method for Energy Optimized Gate Sizing of Digital Circuits, *21st International Workshop, PATMOS 2011 on Power and Timing Modeling, Optimization, and Simulation*, Madrid, SPAIN, September 27, 2011.

[122] Hossein Karimiyan Alidash, Sayed Masoud Sayedi, Vojin G. Oklobdzija, "*Soft-Error Hardened Redundant Triggered Latch*", 4th Asia Symposium on Quality Electronic Design (ASQED), July 10-11, 2012.

[123] V.G. Oklobdzija, M. Aktan, Baran, "*Optimal Transistor Sizing and Voltage Scaling for Minimal Energy use at Fixed Performance*", 7th Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA 2012), Cordoba, Argentina, August 4-12, 2012.

[124] V. Nawathe, M. Aktan, L. Wang, V. G. Oklobdzija, "*Parallelism trade-offs for data-driven circuits*", 7th Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA 2012), Cordoba, Argentina, August 4-12, 2012.

[125] M. Aktan, D. Baran, V.G. Oklobdzija, "*Minimizing Energy by Achieving Optimal Sparseness in Parallel Adders*", 22nd IEEE Symposium on Computer Arithmetic, Lyon, FRANCE, June 22-24, 2015.