VOJIN G. OKLOBDZIJA, Ph.D.

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EXPERT WITNESS PROFILE

Distinguished technical expert with 25+ years of expert witness experience in federal courts, ITC, PTAB, JAMS arbitration, and international proceedings. Has provided testimony in civil jury trials and before judges in the U.S., and delivered tutorials to federal district court judges. Author of 30+ expert reports covering patent infringement, claim construction, invalidity, prior art, and product forensics. Recognized as a leading authority in computer architecture, VLSI design, semiconductor circuits, and digital systems by courts and counsel on both plaintiff and defense sides.

COURT & ARBITRATION TESTIMONY

- International Trade Commission (ITC), Washington D.C., June 5–6, 2013. Two weeks at trial. Case won.
- U.S. District Court, Northern District of California, San Jose. Three days of jury testimony (sole expert vs. half-dozen opposing experts). Case won, October 2, 2013.
- Tutorial to Federal District Court Judge, U.S. District Court, Western District of Texas, Austin Division, August 22, 2019.
- JAMS Arbitration: Red Hydrogen LLC v. CloudMinds (Hong Kong) Ltd., No. 1220062943. Testimony to arbitration judge.

Depositions: 20+ depositions given; most recent three depositions in 2025.

TECHNICAL EXPERTISE

Computer Architecture	Microprocessor design, RISC/superscalar, pipeline, ISA
VLSI Circuits & Systems	High-speed, low-power, clock distribution, custom IC design
Computer Arithmetic	Adders, multipliers, FPUs, crypto processors, floating-point
Semiconductor Systems	Chip design, DFT, fault tolerance, power management, SoC
Clocking & Storage Elements	Flip-flops, latches, clocked logic, multi-GHz systems
Machine Learning Hardware	ML accelerators, datapath, arithmetic units for inference
CAD / EDA Tools	Logic synthesis, timing analysis, IC design automation
Forensic Analysis	Reverse engineering, product failure analysis, IP identification

LITIGATION SUPPORT HISTORY (SELECTED)

Date	Law Firm	Representing	Subject / Status
2022–25	**Hagens Berman / Bathaee Dunne**	Plaintiffs	Defective product
2022–25	**Devlin Law Firm LLC**	Plaintiff	Patent infringement (10 patents)
2022–24	**Hundel Law Group**	VOIP-PAL.com	Patent infringement
2023–24	**Covington & Burling LLP**	Samsung	Prior art search / consulting
2023	**Jones Day / Knobbe Martens**	Qualcomm	IPR; prior art; technology
2023	**Simon Law Group**	Plaintiff	Product forensics
2021–23	**Winston & Strawn LLP**	Micron	Patent / IPR
2021	**Dhillon Law Group**	Cryplex	Trade secret / IP identification
2021	**Cesari and McKenna LLP**	FrontierLabs	Non-infringement analysis
2020	**Di Muro Ginsberg P.C.**	SRC LLC	IPR / patent review
2020	**Weeks Nelson LLP**	Red Hydrogen	Mobile phone manufacturing
2019	**Freitas & Weinberg LLP**	Plaintiffs	Patent infringement (3 reports)
2019	**Antonelli Harrington & Thompson**	American Patents	Patent infringement / claim construction
2018	**Morrison & Foerster LLP**	Ubiquiti	EDA tool usage
2017	**Bunsow de Mory LLP**	TPL	Chip clocking
2016–17	**Freitas Angell & Weinberg**	Broadcom/Avago	Patent / prior art
2015–16	**Desmarais LLP**	IV LLC	On-chip testability / DFT
2015–16	**Farney Daniels PC**	Memory Integrity	Cache coherency (multiprocessor)
2015	**Latham & Watkins LLP**	Nvidia	Display power-down technology
2015	**Nelson Bumgardner P.C.**	TPL	Microprocessor clocking
2015	**Arnold and Porter LLP**	Atop Tech	IC timing simulation / CAD
2015	**AZA Law**	Parthenon UMA	Mobile chip shared memory
2012–14	**Otteson Law / Agility IP**	TPL	Microprocessor clocking
2012	**Wolf Greenfield & Sacks**	Graphics Properties	Microprocessor clocking
2012	**Irell & Manella LLP**	Atmel	Thermal/power management
2011	**Arnold and Porter LLP**	HP	IC low-voltage / power management
2009	**DLA Piper US LLP**	Zoran	DTS algorithm / reverse engineering
2008–11	**Farella Braun + Martel LLP**	TPL	Microprocessor clocking
2008–09	**Nixon Peabody / Thelen LLP**	TPL	Microprocessor architecture

2008–09	**Townsend Townsend & Crew**	TPL	Asynchronous clocking
2007–08	**Dechert LLP**	HP	Microprocessor clocking
2007	**Townsend Townsend & Crew**	TPL	Computer circuits; asynchronous clocking
2004–06	**Kellogg Huber Hansen Todd & Evans**	OKI	Patent invalidity; expert report
1999–00	**Townsend Townsend & Crew**	Sun Microsystems	Computer circuits and logic
1997–98	**Bernstein Litowitz Berger & Grossmann**	Plaintiffs	AMD K5 processor design / project mgmt

EDUCATION

Ph.D., Computer Science (1982)	University of California, Los Angeles | Minor: Electronics & DSP
M.S., Computer Science (1978)	University of California, Los Angeles | Thesis: Arithmetic Processor Design
M.S.E.E. & B.S.E.E. (1971)	University of Belgrade, Yugoslavia | Electronics & Telecommunications

CREDENTIALS & RECOGNITION

- IEEE Life Fellow (2016) — the highest IEEE grade; only 3,517 of 427,000 members worldwide
- IEEE Fellow (1996) — fewer than 0.1% of members elected annually
- President, IEEE Circuits and Systems Society (2014–2016)
- Distinguished Lecturer, IEEE Solid-State Circuits Society (2000–2006) and IEEE CAS Society
- Fulbright Scholar (1976–77); Fulbright Professor, Peru (1991) and Argentina (2013)
- Outstanding Academic Title: “Computer Engineering Handbook,” CRC Press 2002 (selected from 22,000 titles by Choice Magazine)
- Best Paper Award, 21st Hawaii International Conference on System Sciences (HICSS-88)
- IBM Patent Award & Invention Plateau Award (1985)
- Listed in Marquis ‘Who’s Who in America’ and ‘Who’s Who in Science and Engineering’

PROFESSIONAL EXPERIENCE (SELECTED)

2018–2023	Senior Principal Engineer, SambaNova Systems Inc., Palo Alto, CA ML supercomputer (Stanford-based; $1.5B funding from Alphabet, Intel, Softbank). Led FPU development achieving 3× performance improvement. 8 patents issued.
2016–2018	Founding Member, Esperanto Technologies, Mt. View, CA Ultra-low-power RISC-V massively parallel ML processor.
1996–Present	President & CEO, Integration Corp., Berkeley, CA Consulting and chip design services. Developed fastest network encryption processor for Blue Steel Networks (acquired by Broadcom for $150M).

1991–2006	Full Professor (now Emeritus), UC Davis — Dept. of ECE Reached Full Professor in 5 years. Founded ACSEL Laboratory.
2005–2007	Chair Professor, University of Sydney, Australia (ARC grant: $1.9M)
1996–1998	Architecture / Circuit Design Manager, Siemens Corp., San Jose Chief architect, Siemens/Infineon TriCore RISC-DSP; managed 15 engineers.
1997–2001	Consultant – Architect & Project Leader, SONY LSI Systems Labs, San Jose Led new generation media processor; reported to Sony Corp. VP.
1982–1991	Research Staff Member, IBM T. J. Watson Research Center, Yorktown Heights VLSI RISC development: 801 (PC-RT), RS/6000 FP processor (PowerPC), IBM SP-2.
1988–1990	Visiting IBM Faculty, UC Berkeley EECS Taught CS150, CS152, CS252. Assisted in review of Patterson-Hennessy textbook.

PUBLICATIONS SUMMARY

224 total publications • h-index: 46 • 8,238+ citations (Google Scholar) • i10-index: 112
6 Books • 11 Book Chapters • 43 Journal Papers • 124 Conference Papers • 222 Presentations

- V. G. Oklobdzija, “High-Performance System Design: Circuits and Logic,” IEEE Press, 1999.
- V. G. Oklobdzija, “Computer Engineering,” CRC Press, 2001. [Outstanding Academic Title 2002]
- V. G. Oklobdzija et al., “Digital System Clocking: High-Performance and Low-Power Aspects,” Wiley, 2003.
- V. G. Oklobdzija & R. K. Krishnamurthy, “High Performance Energy Efficient Microprocessor Design,” Springer, 2006.
- V. G. Oklobdzija, “Digital Systems and Applications,” Taylor & Francis, 2007.
- V. G. Oklobdzija, “Digital Design and Fabrication,” Taylor & Francis, 2007.

U.S. PATENTS (RECENT)

Patent No.	Issued	Title
12,417,078 B2	Sep. 16, 2025	Floating-Point Accumulator with a Single Layer of Shifters in the Significand Feedback
11,983,509 B2	May 14, 2024	Floating-Point Accumulator
11,967,955 B2	Apr. 23, 2024	Fast Clocked Storage Element
11,831,316 B2	Nov. 28, 2023	System of Free Running Oscillators for Digital System Clocking Immune to PVT Variations
11,558,041 B1	Jan. 17, 2023	Fast Clocked Storage Element
11,442,696 B1	Sep. 13, 2022	Floating Point Multiply-Add, Accumulate Unit with Exception Processing
11,429,349 B1	Aug. 30, 2022	Floating Point Multiply-Add, Accumulate Unit with Carry-Save Accumulator
11,366,638	Jun. 21, 2022	Floating Point Multiply-Add, Accumulate Unit with Combined Alignment Circuits
10,707,839	Jul. 7, 2020	System of Free Running Oscillators for Digital System Clocking Immune to PVT Variations
7,509,486	Mar. 24, 2009	Encryption Processor for Performing Accelerated Computations to Establish Secure Network Sessions
6,753,715	Jun. 22, 2004	System for Symmetric Pulse Generator Flip-Flop

6,353,843	Mar. 5, 2002	High Performance Universal Multiplier
4,992,398	Feb. 12, 1991	Instruction Control Mechanism for a Computing System with Register Renaming and Queues
4,847,759	Jul. 11, 1989	Register Selection Mechanism and Organization of an Instruction Prefetch Buffer
4,714,994	Dec. 22, 1987	Instruction Prefetch Buffer Control

Also holds European, Japanese, and WIPO patents. Full patent list available at www.acsel-lab.com.

References and complete curriculum vitae available upon request • www.integration-corp.com